VLSI Architectures for Digital Signal Processing on Energy Constrained Systems-on-Chip

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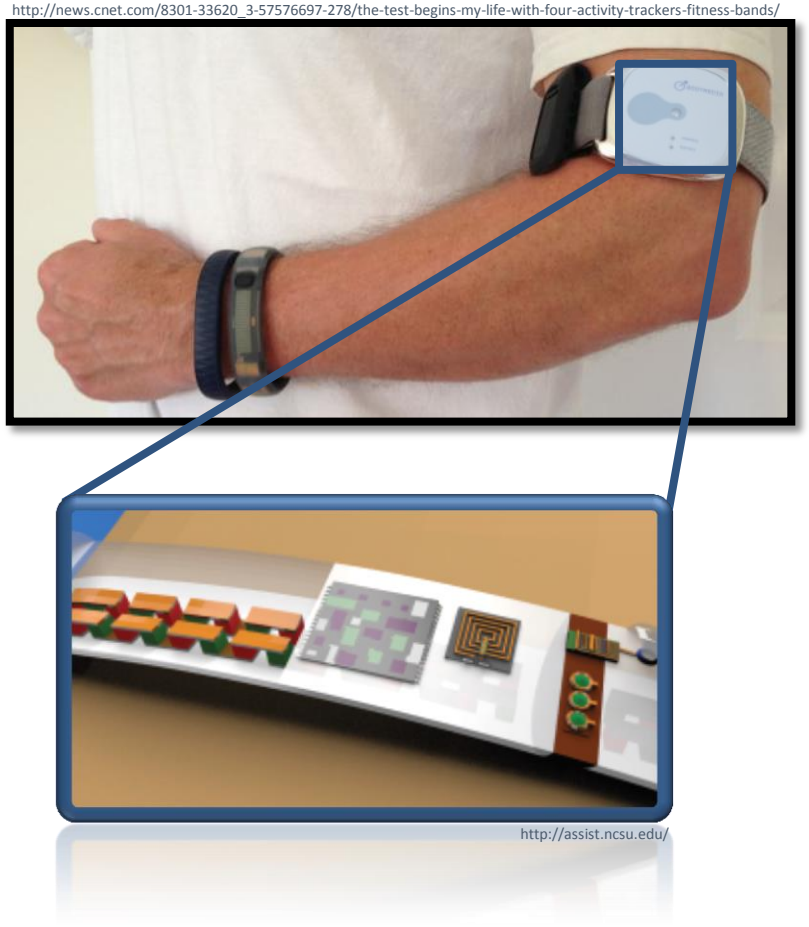
Robust Low Power VLSI

Motivation

- Systems-on-Chip (SoCs) for biomedical applications are an emerging field
  - Ubiquitous computing
  - Body Sensor **Nodes** (BSNs)
- Requirements:
  - Unobtrusive monitoring
  - Long lifetimes
- On-chip processing
  - Low average power (30-50μW)
  - Accurately extract physiological data

http://news.cnet.com/8301-33620_3-57576697-278/the-test-begins-my-life-with-four-activity-trackers-fitness-bands/



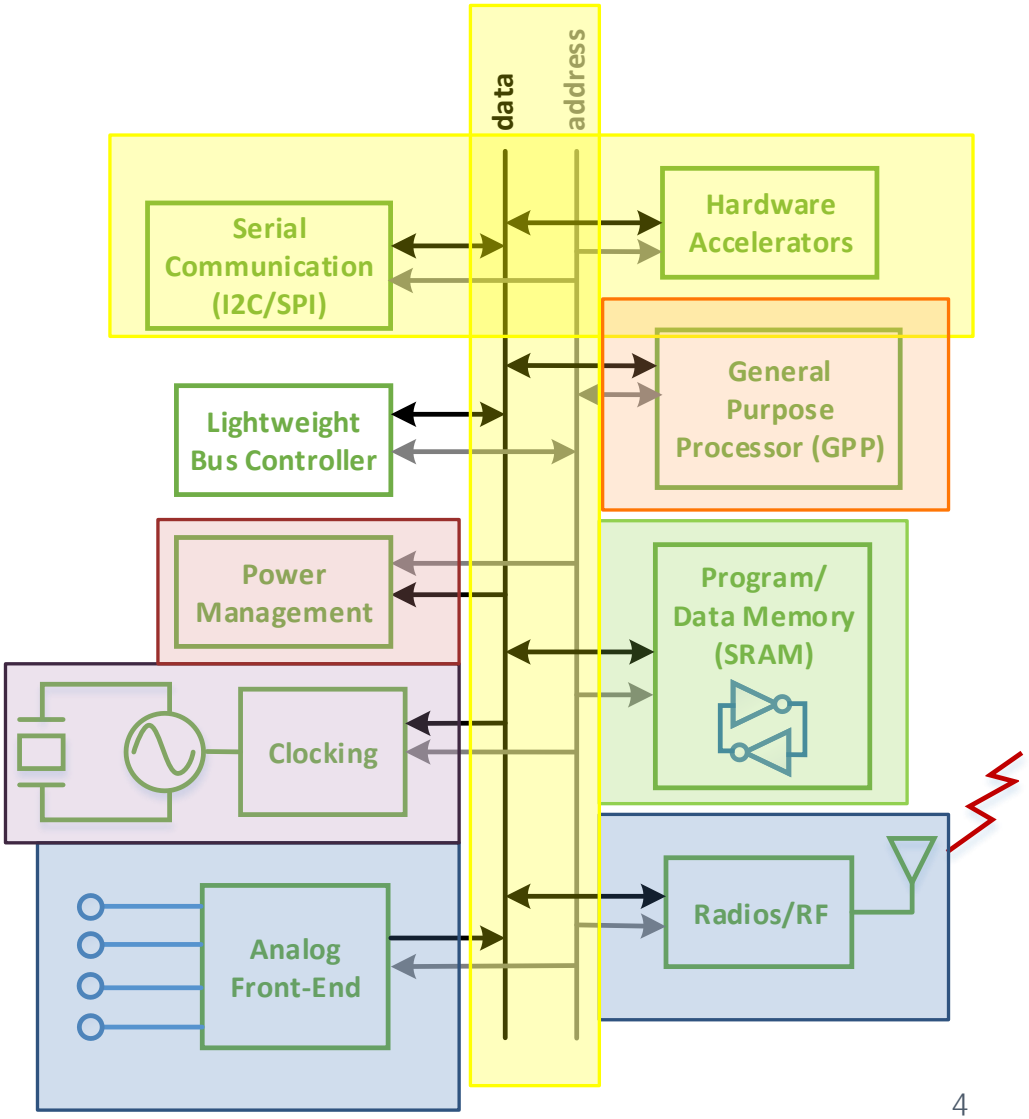
http://assist.ncsu.edu/

Outline

1. Motivation and Introduction
    1. Body Sensor Nodes (BSNs)
    2. Energy Constrained SoCs
    3. Thesis and Research Goals
2. Subthreshold Digital Signal Processing (DSP)
    1. Finite-Impulse Response (FIR) Filter
    2. Fast-Fourier Transform (FFT)
    3. Approximation Techniques for FIR filter coefficients
3. **S**oC **U**ltra-Low **P**owe**R** (SUPR) Model
    1. All-Digital Phase Locked Loop (ADPLL) for clock synthesis and model validation
4. Schedule
5. Publications

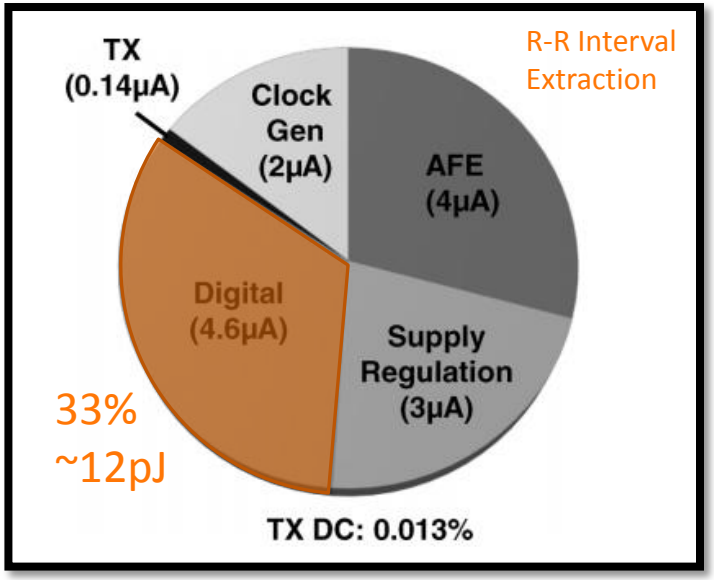
SoC Architecture

- Packaging of many electronic circuits on a single integrated circuit
  - General Purpose Processor (GPP)
  - Peripherals
    - Accelerators
    - External Interfaces
  - Analog Interfaces
  - Clocking
  - Memory
  - Power Management
- Blocks connected by bus
- Battery → Energy constrained



BSN Energy Minimization

- Digital consumes 33% of on-chip BSN current
  - Large portion memory and accelerators
    - FIR > 4x more energy
  - Room for improvement and impact
- Challenges
  - GPP versus accelerators
  - Application space limitations
- Approach
  - Subthreshold operation
  - Digital block-level architecture modifications

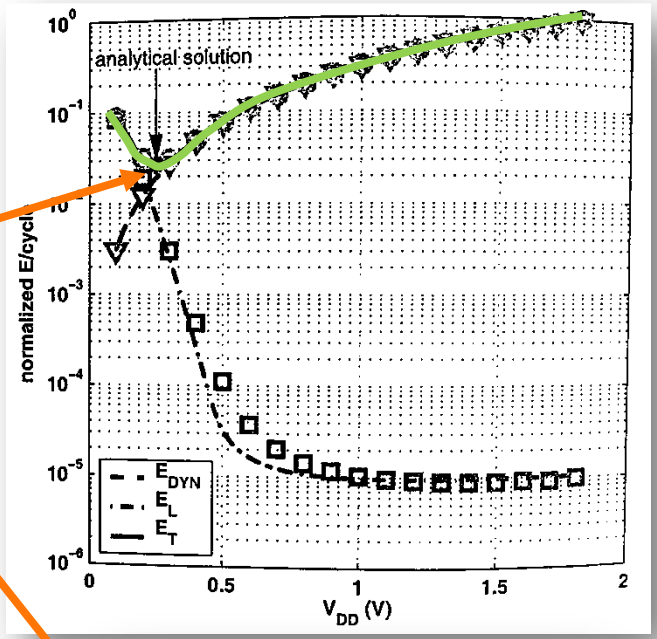


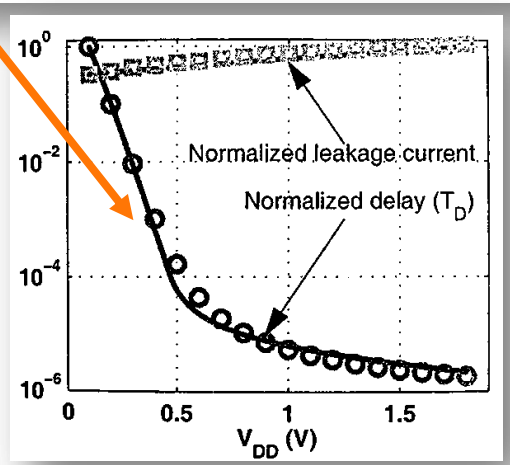
Energy Efficiency Comparison Per Sample		
30 Tap FIR	GPP	6.3 nJ
	Accel	**57pJ**
Signal Energy Extractor	GPP	3.6 nJ
	Accel	530 fJ
R-R Interval Extractor	GPP	12 pJ
	Accel	3 fJ

Zhang, F., et. al "A Batteryless 19uW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", ISSCC, San Francisco, 02/2012.

Subthreshold Operation

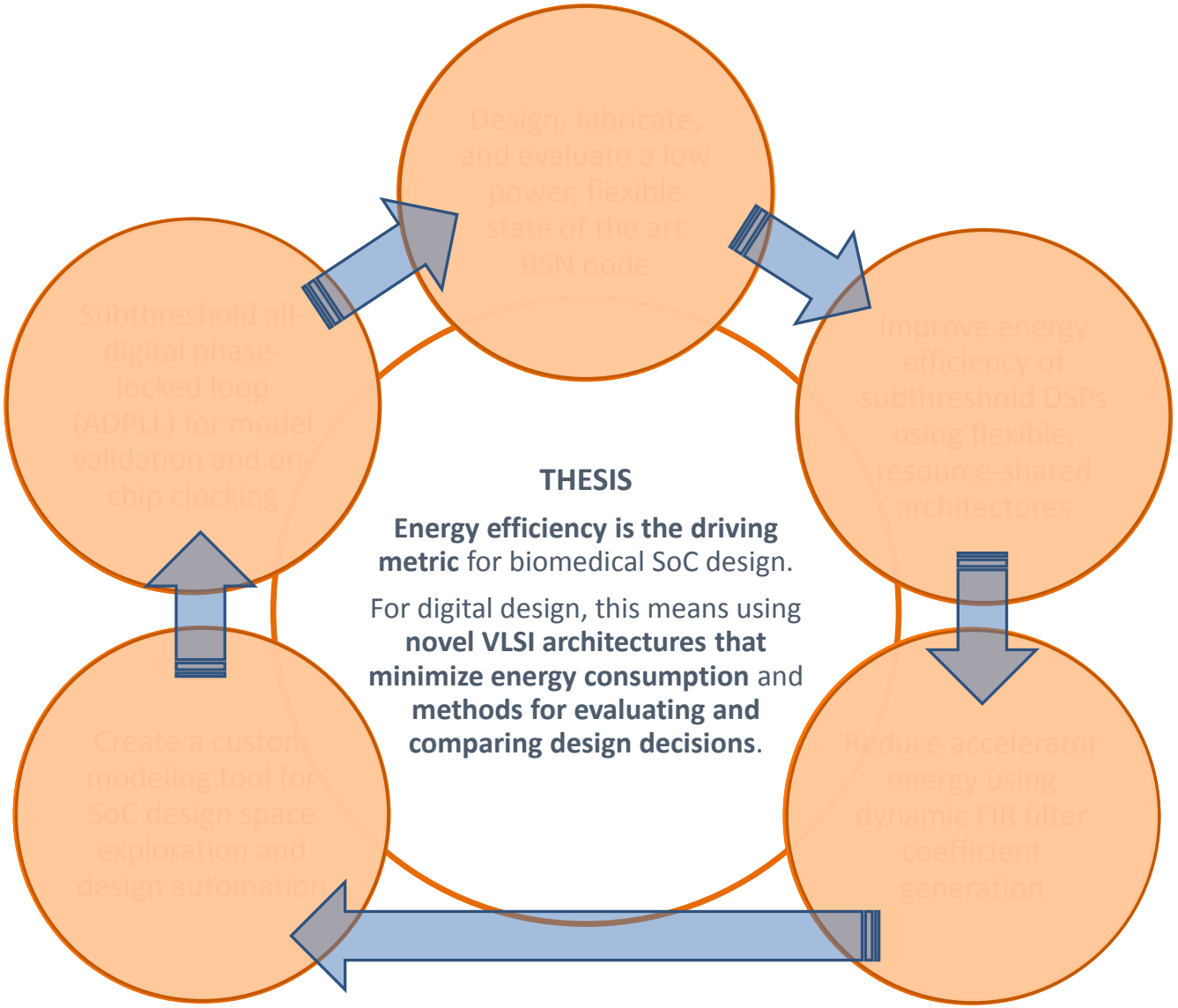
- Operate below devices' threshold voltage
  - Minimizes energy per operation
- Quadratic energy reduction
- Exponential performance penalty
- Design Challenges
  - Meeting throughput constraints
  - Synthesis for subthreshold
- Further energy reductions
  - Modify block topology





Alice Wang, Benton H. Calhoun, and Anantha Chandrakasan. Sub-threshold Design for Ultra Low-Power Systems. Springer, 2006.

Thesis and Goals



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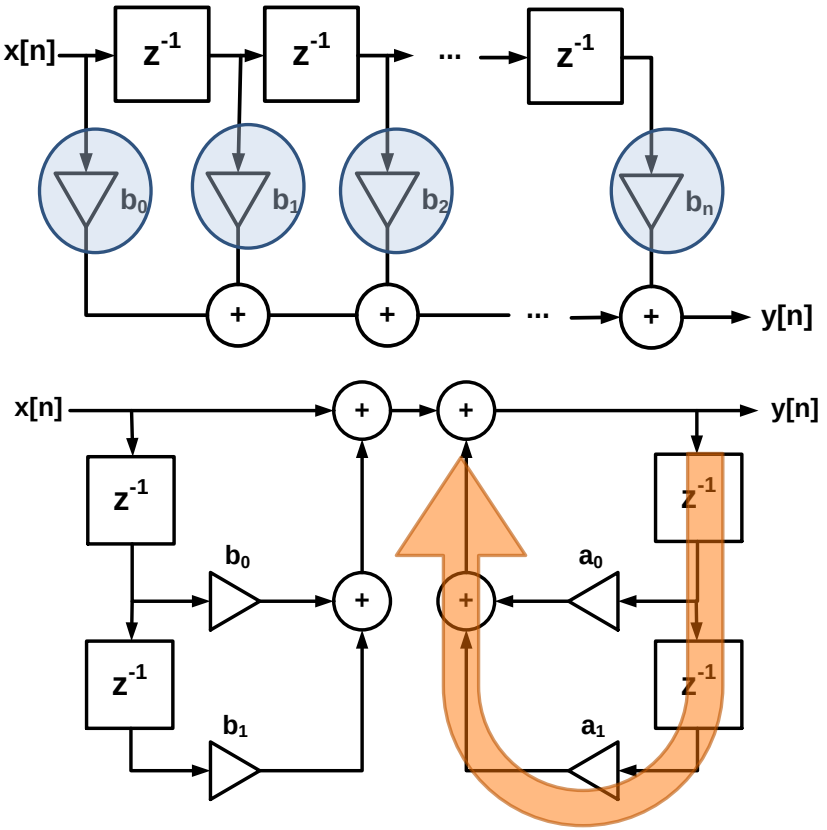
Motivation and Overview

- Filtering frequently used for power spectral analysis on BSN
- Finite-Impulse Response (FIR) vs. Infinite-Impulse Response (IIR)
  - Feedback (instability)
  - Transition and roll-off sharpness
- Direct-mapped filtering:
  - More Taps → higher accuracy, *and* power



Hypothesis and Metrics

Hypothesis

1. BSN applications require accurate filtering at a variety of bandwidths.
2. **Directly mapping traditional DSP algorithms to hardware leads to suboptimal designs** if energy is the driving metric.
3. **Serializing DSP architectures can drastically reduce area and energy** while still meeting the throughput demands for a variety of BSN applications.

Neurological State	Frequency Band
Visual processing/motor planning	8-12Hz (α)
Awake and alert	18-26Hz (β)
Consciousness/Awareness (Present)	70-100Hz (γ)
Consciousness/Memories (Past)	30-50Hz (low-γ)
Light Sleep	4-7Hz (θ)
Deep Sleep	0.5-3Hz (δ)

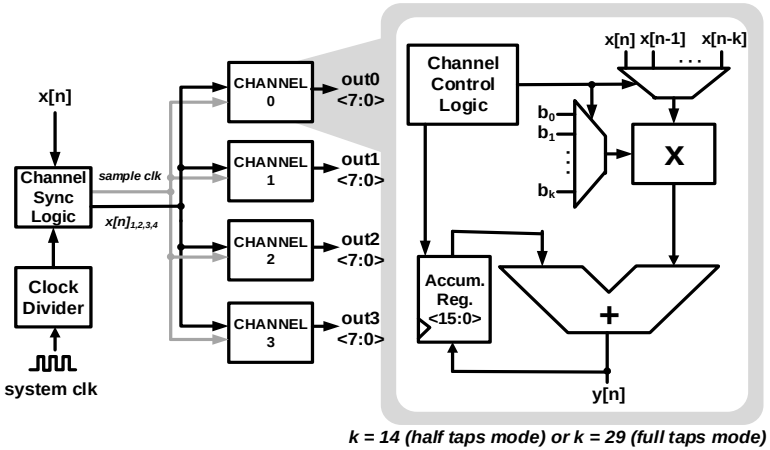
Metrics

- Programmability
- Energy/Tap versus Supply Voltage
- Frequency versus Supply Voltage
- Active and leakage energy
- Area

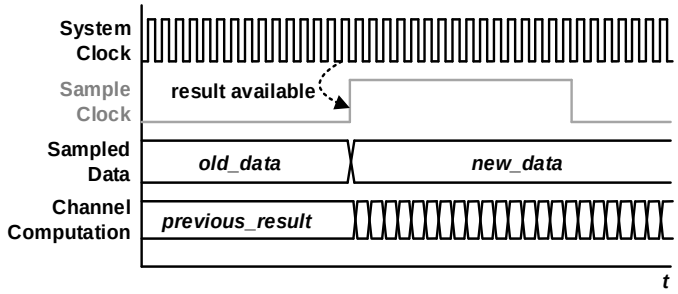
Klinefelter, A.; et al, "A Programmable 34 nW/Channel Sub-Threshold Signal Band Power Extractor on a Body Sensor Node SoC," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.59, no.12, pp.937,941, Dec. 2012.

Approach

- Four input channels (ExG front-end)
- Resource-shared architecture
  - Minimized area, leakage
- Programmable
  - Coefficients
  - Taps
  - Active Channels



k = 14 (half taps mode) or k = 29 (full taps mode)



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Results and Comparison

- Lowest energy/area, best figure of merit (FOM)
- Completely synthesizable using standard cells
- Next iteration: flexible taps, channel daisy-chaining

	This Work	[6]	[7]	[8]
Type	30-tap, 8-bit	8-tap, 8-bit	14-tap, 8-bit	4th order analog
Channels	4	1	1	4
Programmable	✔	✕	✕	✔
Technology	0.13µm	0.13µm	0.13µm	0.13µm
Supply Voltage	350mV	200mV	270mV	1.2V
Frequency	29kHz	12kHz	20MHz	20kHz
Energy/Tap	1.10pJ	1.19pJ	1.11pJ	(total) 39pJ
Power	32nW	114nW	310µW	780nW
FOM*	0.57	18.55	17.37	N/A
Area/Channel	0.058mm^2	1.54mm^2	0.38mm^2	0.7mm^2

*FIR FOM: power(nW)/frequency(MHz)/# of taps/input bit length/coefficient bit length.

Klinefelter, A.; et al, "A Programmable 34 nW/Channel Sub-Threshold Signal Band Power Extractor on a Body Sensor Node SoC," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.59, no.12, pp.937,941, Dec. 2012.

FIR Contributions

1. Completed analysis for most reliable filtering topology
    1. Reliability–Accuracy tradeoff
2. A fabricated and tested multi–channel subthreshold FIR filter with the best FOM in its class
3. Determine benefits of flexible taps and channel “daisy–chaining”
    1. Flexibility – Power Overhead

Outline

1. Motivation and Introduction
   1. BSN Chip
   2. Subthreshold Operation
   3. Research Goals
2. Subthreshold DSPs
   1. Finite-Impulse Response (FIR) Filter
   2. Fast-Fourier Transform (FFT)
   3. Approximation Techniques for FIR filter coefficients
3. SoC Ultra-Low PoweR (SUPR) Model
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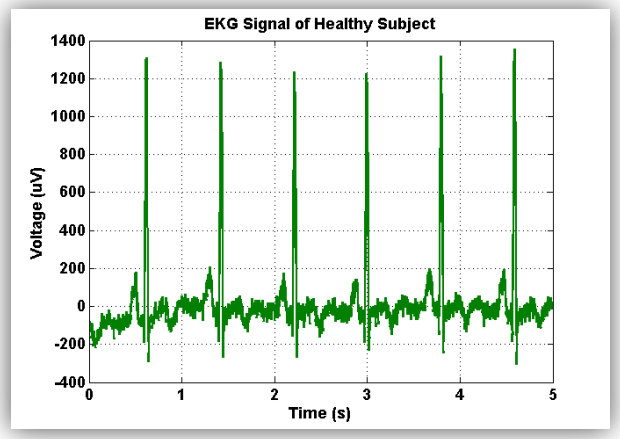
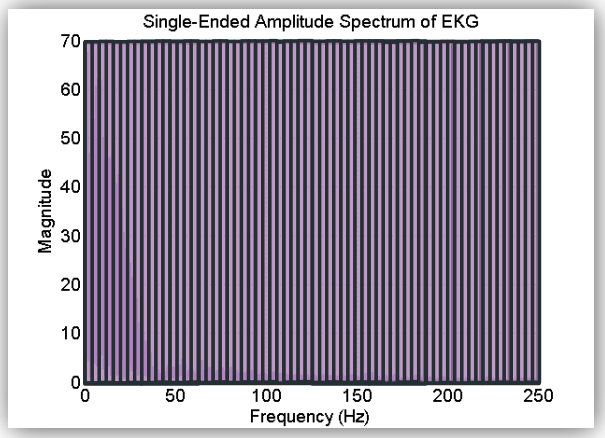
FFT Motivation

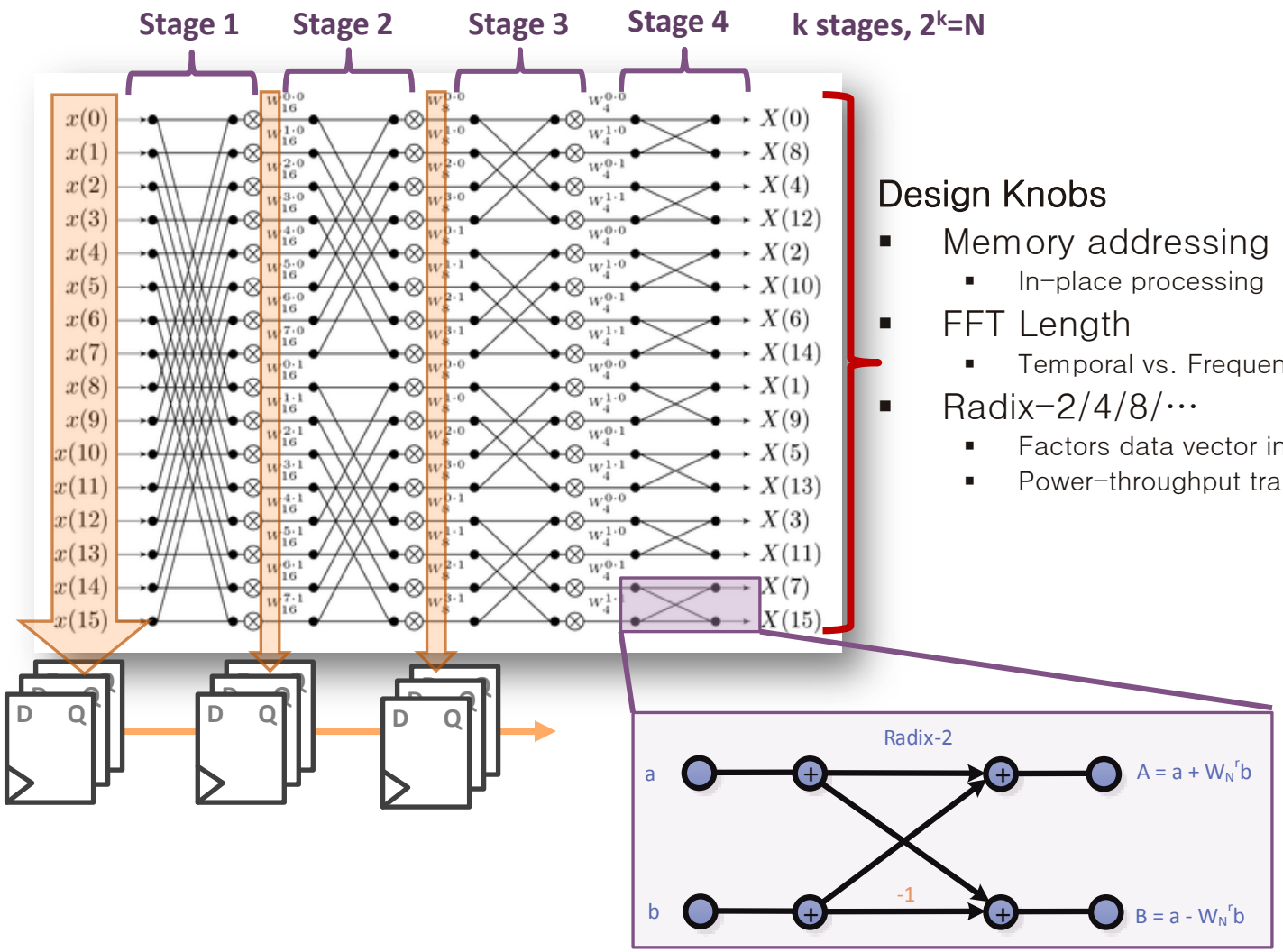
- Frequency domain analysis frequently used in BSNS
  - Sensor Signal Processing (Classification)
- FFT pitfalls
  - Memory intensive
  - Large runtime $O(n\log_2(n))$
  - One size does not fit all applications



$$\xrightarrow{FFT} \quad X(k) = \sum_{n=0}^{N-1} x[n] e^{\frac{-j2\pi kn}{N}}$$



FFT Overview



Design Knobs

- Memory addressing schemes
  - In-place processing
- FFT Length
  - Temporal vs. Frequency resolution
- Radix-2/4/8/…
  - Factors data vector into shorter lengths
  - Power-throughput tradeoff

http://www.texample.net/tikz/examples/radix2fft/

Hypothesis and Metrics

HYPOTHESIS

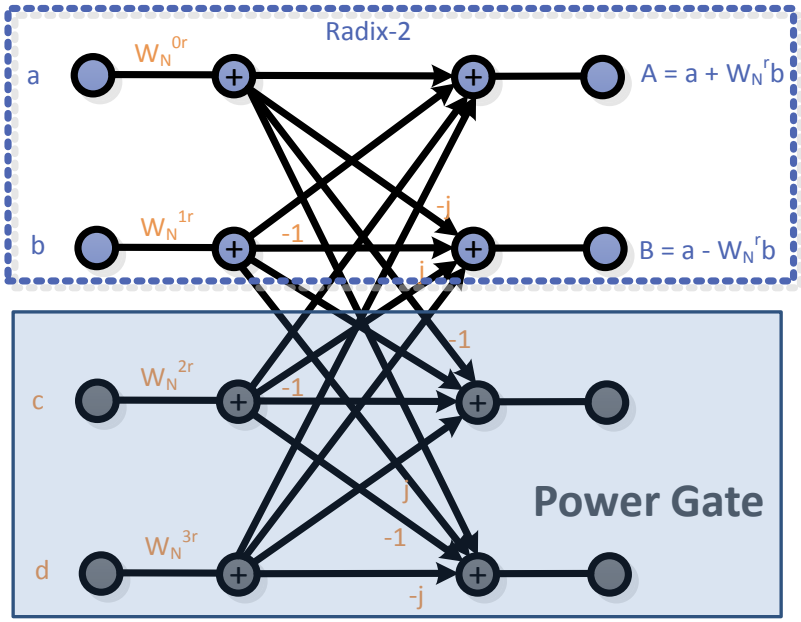
1. FFTs are very memory intensive for a large N. **Reducing memory/storage** used by this circuit will improve robustness and reduce area.
2. **Increase flexibility across the application space** using a mixed-radix design.
3. Reduce energy by **only computing/storing required results**, and using real-valued inputs.

METRICS

- Programmability
- Energy/Sample versus Supply Voltage
- Frequency versus Supply Voltage
- Active and leakage energy
- Throughput
- Area

Approach

- Remove twiddle ROM
- Mixed-radix for improved throughput
  - Radix-2 and 4 Stages for improved flexibility
    - New memory addressing scheme required
    - Energy efficient multi-port adders
  - Power gate radix-4 components when not used
- Use fine-grained clock gating controller
  - Inactive registers
  - Unused butterfly elements



FFT Contributions

1. Fabricated subthreshold 64-point, radix-2 FFT for a BSN node
2. Improve subthreshold FFT structures and control logic for flexible processing
    1. Remove twiddle ROM to improve robustness and reduce area
    2. Only use low-area standard cell registers
    3. Reduce energy by only storing selective outputs, using fine-grained power gating
    4. Improve flexibility using mixed-radix design and supporting input array shifting for short-time FFT

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Overview

- Subthreshold SRAM
  - Leaky
  - Not robust in subthreshold
    - Ratioed circuit → Sensitive to variations
  - Custom design
- Coefficients stored in data memory (SRAM) or local register file
- Program by wireless on BSN
  - Limit the size of the payload

Hypothesis and Metrics

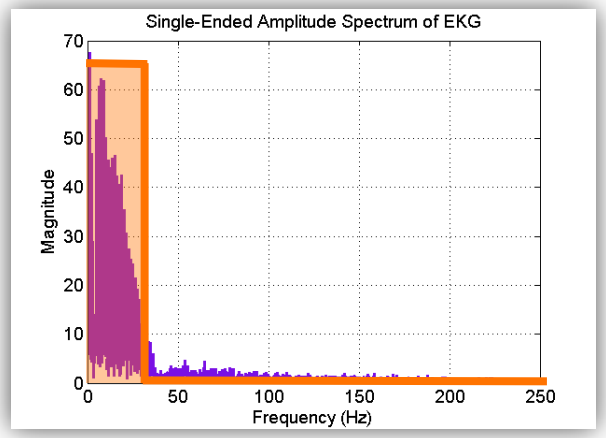
HYPOTHESIS

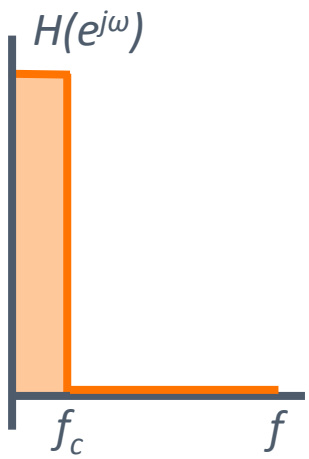
1. **Dynamically generating filtering coefficients** on chip using approximation methods **can lead to more robust, low power operation** on BSN nodes.
2. Filters requiring a large number of taps can benefit the most from this approach due to **reduced reliance on subthreshold SRAMs for storage.**

METRICS

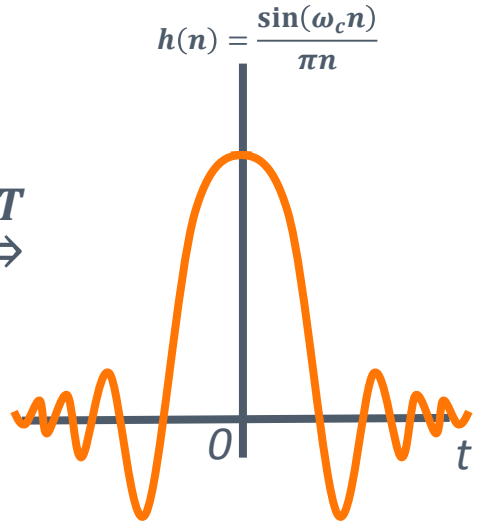
1. Energy
2. Number of arithmetic resources
3. **Robustness (at low voltages)**
4. Area with respect to taps
5. Throughput

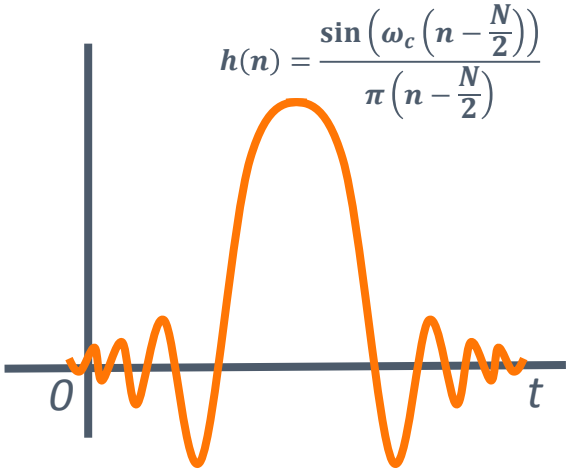
Approach

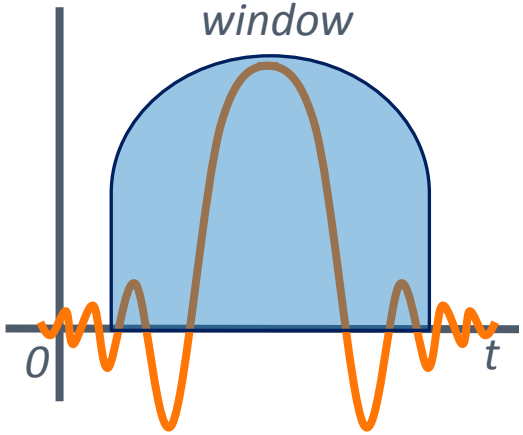


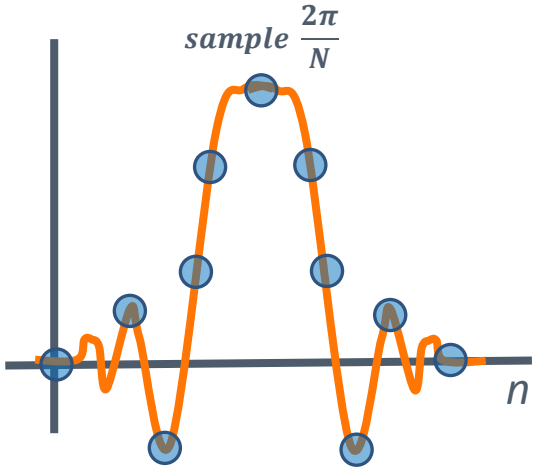


$$IDTFT \Longrightarrow$$









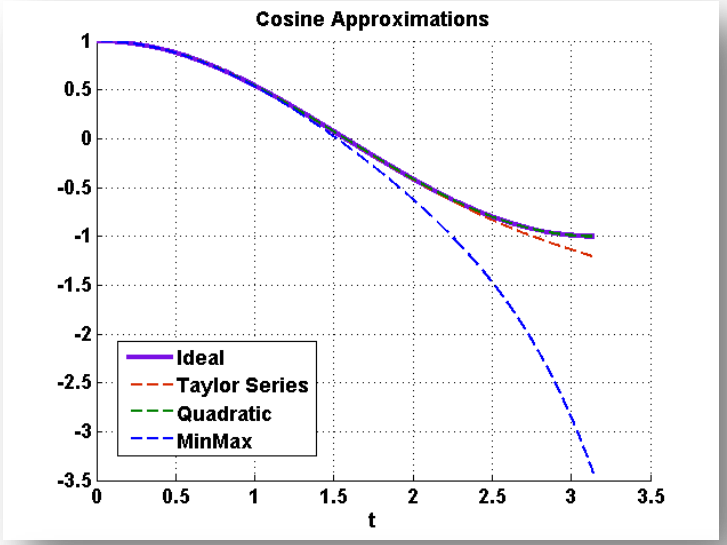
Approach Reiterated

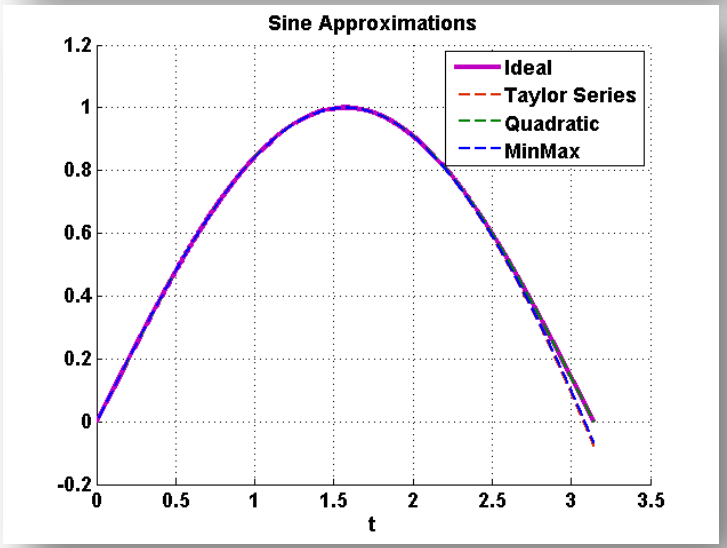
1. Define filter specifications
    1. Cutoff/stopband frequencies
    2. Windowing function
    3. Filter order
2. Generate an ideal impulse response function
3. Multiply the sinc function by the specified window and sample to obtain coefficients.

Rectangular	$w[n] = 1$
Bartlett	$w[n] = 1 - \frac{\lvert n \rvert}{N+1}$
Hamming	$w[n] = 0.54 + 0.46\,cos\left(\frac{2\pi n}{2N+1}\right)$

Approximation Methods

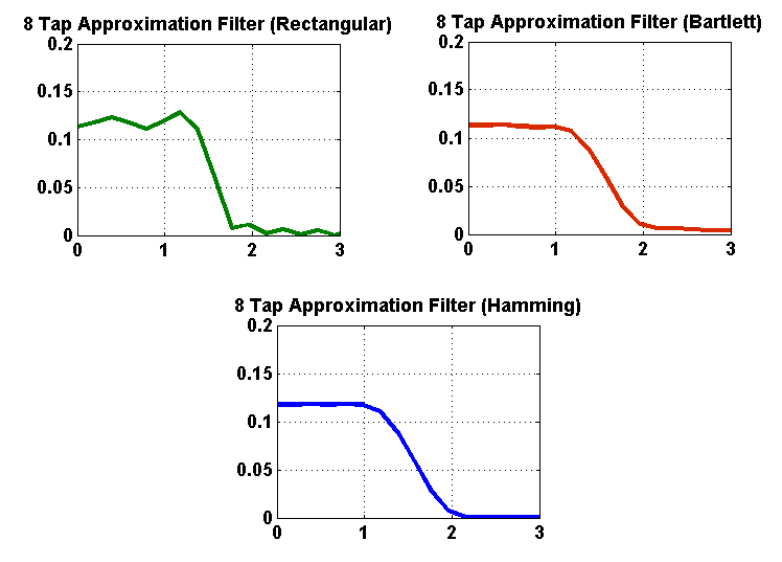
- Three approximation methods examined:
  1. Taylor Series
  2. Quadratic
  3. MinMax polynomials
- Sinc approximations



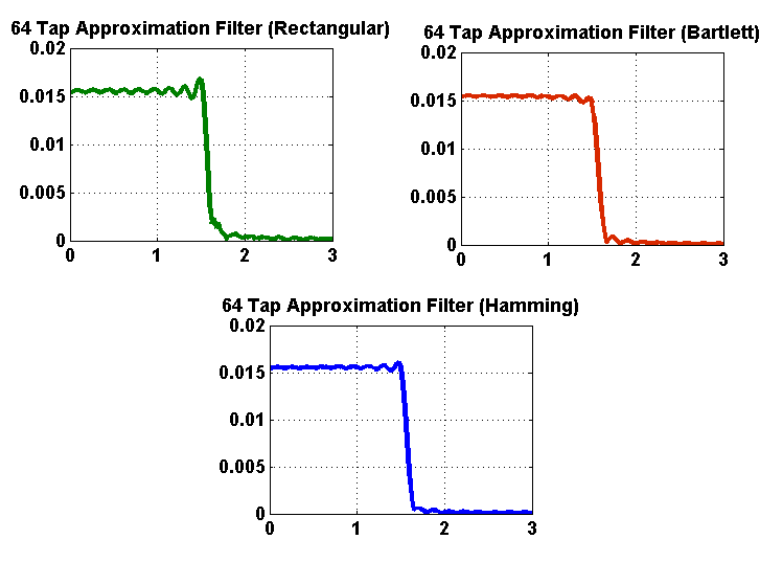


Preliminary Results

8-tap Approximation



64-tap Approximation

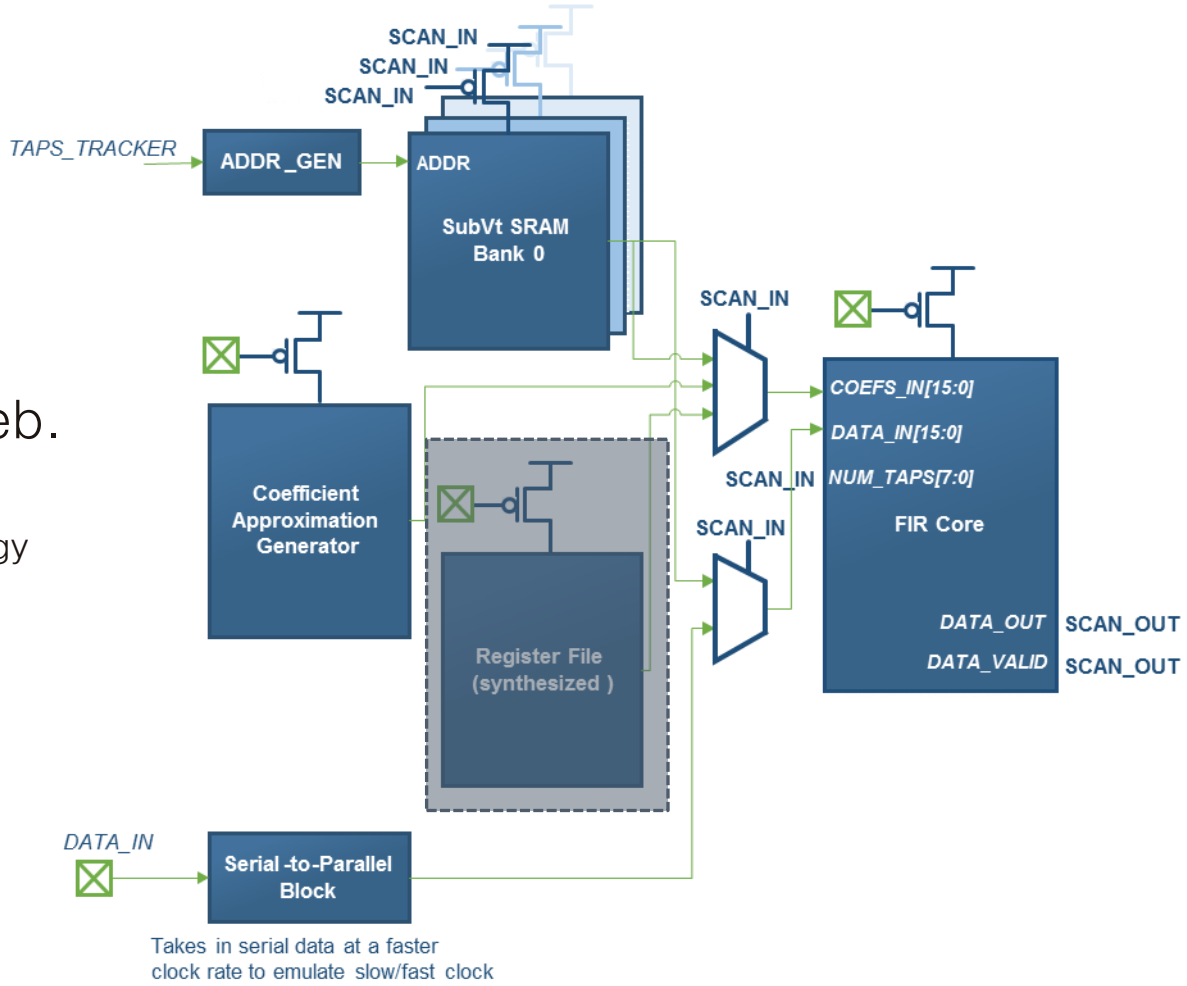


- Approximation for 64-tap filter:
  - Area: 250 μm x 250μm
  - Active energy: 20fJ, leakage energy of 0.75fJ
- SRAM (4kB)
  - Area: 780 μm x 770μm
  - Active energy: 24.2fJ, leakage energy of 13.18fJ

The approximation method results in lower energy, but still falls short in area and throughput for small taps.

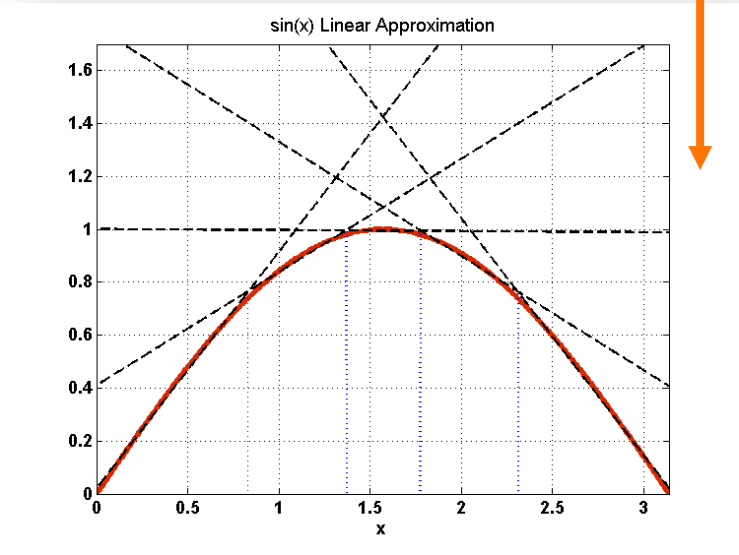
Approximation Test Design

- Test design fabricated in Feb. 2013
  - 130nm technology



DSP Approximation Contributions

- Trigonometric function approximation comparison
  - Arithmetic Resources –Accuracy
- Coefficient Approximation Methodology
- Fabricated Test Chip
  - Accuracy–energy –Area
- Determine application limitations of using this method for filtering
- Reduce energy by applying to FFT twiddle factors
  - Reduce memory
  - Aggregate area/energy cost of approximation



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SUPR Motivation

- High SoC integration density and complexity
  - Determining bottlenecks early in design process
- Evaluating tradeoffs difficult
  - Design and simulation time
  - Cost ($)
- Don't want to burden the designer
  - New tools
  - More steps to design process

Automate and **accelerate** the design comparison process

SUPR Overview

- Tool designed using MATLAB and Simulink
  - Industry standard for signal processing
- Simulink Hardware Support
  - HDL Co-simulation with ModelSim
  - Stateflow and HDL Coder tools
  - Custom library design support
- Answer component and system-level design questions
- Provide a link between high-level algorithm description and hardware tradeoffs

Hypothesis and Metrics

HYPOTHESIS

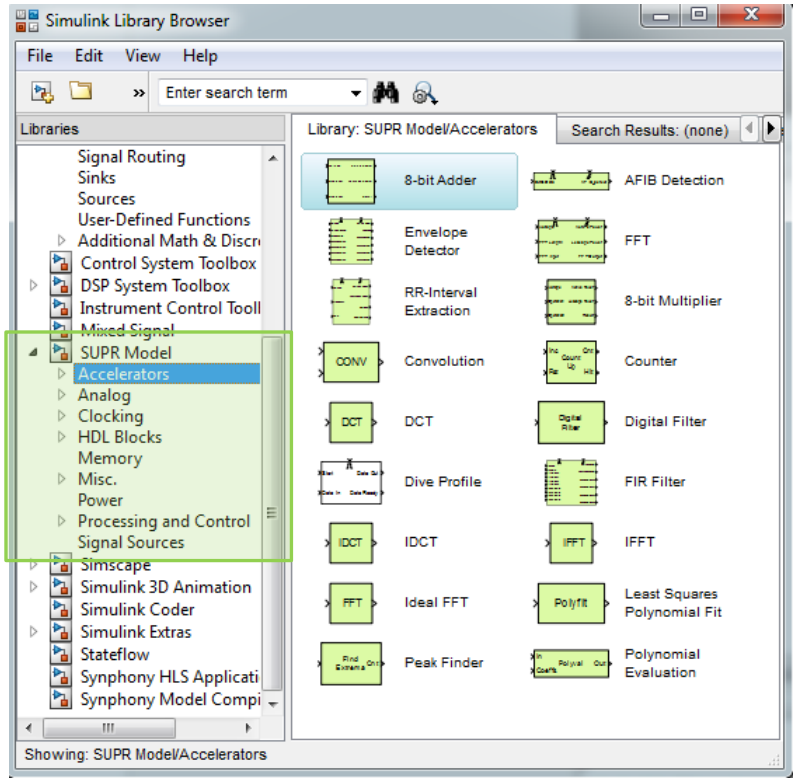
1. SUPR provides a **scalable component-level library**
2. SUPR will aid in **justifying architecture-level design decisions** for quick comparisons to design alternatives
3. SUPR will **form a full design loop** between high-level algorithm description and physical design evaluation

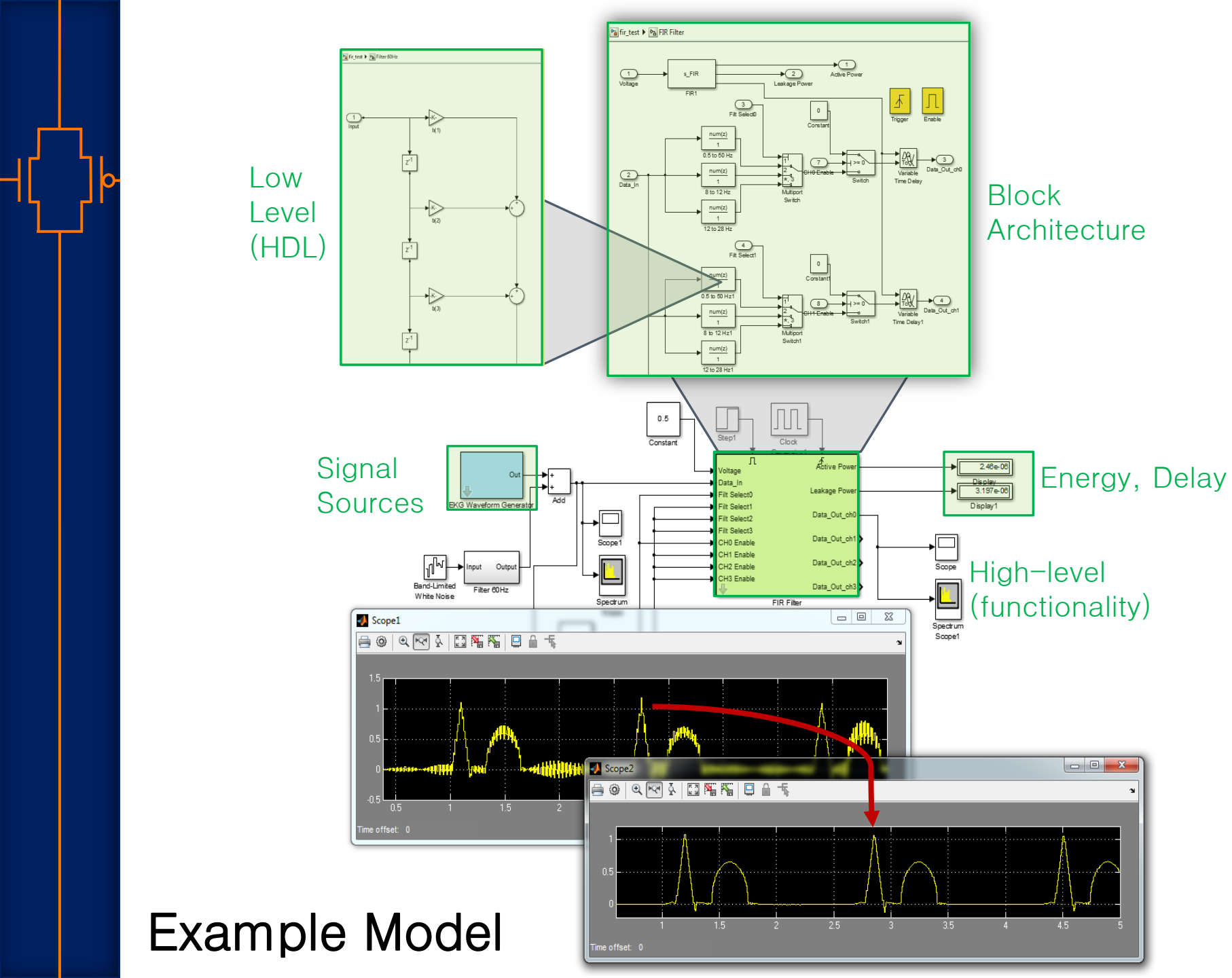
METRICS

1. Accuracy compared to SPICE
2. Simulation time speedup
3. Level of Abstraction
4. Ease of Use
    1. Interface
    2. Automation without interference

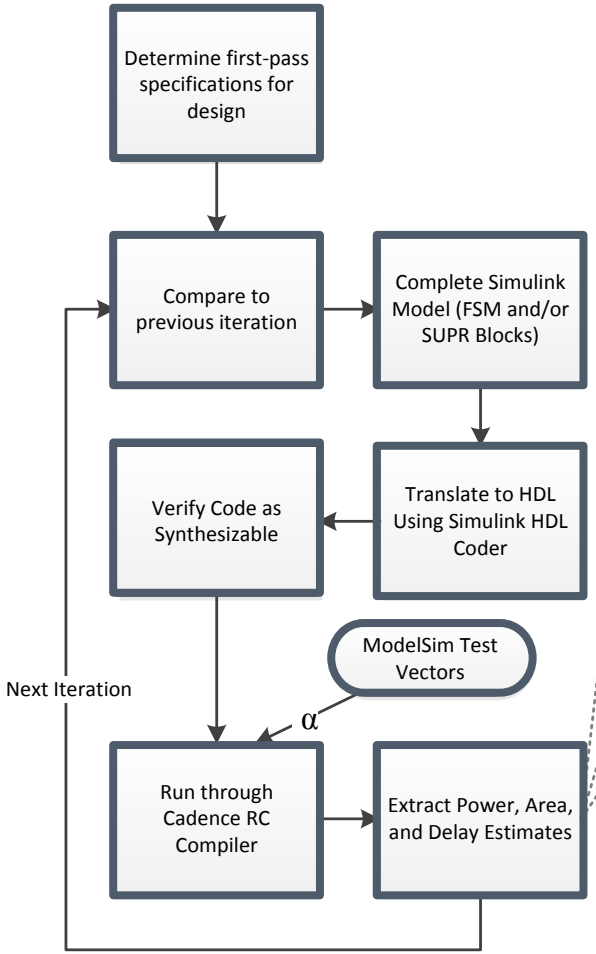
Approach

- Library of SoC system blocks
- Digital representation:
  - Energy, delay
  - High and low-level descriptions
- Analog/Mixed-Signal/RF:
  - Energy, delay (interpolated)
  - High-level behavior




Low Level (HDL)
Block Architecture
Signal Sources
Energy, Delay
High-level (functionality)
Example Model
FIR Filter
Scope1
Scope2
Time offset: 0
Time offset: 0

Design Automation Approach



Type	Instances	Area	Area %
sequential	**1789**	**58203.360**	**45.4**
inverter	191	825.120	0.6
tristate	257	4070.880	3.2
logic	**4668**	**64967.040**	**50.7**
total	6905	128066.400	100.0

Instance	Cells	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)
fir_top	**6905**	**700.259**	**16346.410**	**17046.669**
fir_decoder	**492**	**348.452**	**5838.467**	**6186.920**
fir_core	**6286**	**347.022**	**9194.028**	**9541.050**
ch0_mac	595	44.965	228.779	273.743
fir_mult	502	37.040	42.875	79.915
invert_and..11_adder15_15	4	0.163	1.934	2.097
I3	1	0.138	1.663	1.800

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
fir_config_reg							
block_config_reg_5/CK				1000		0	R
block_config_reg_5/Q	DFFSHQX1TS	4	6.9	10183	+28532	28532	R
g456/A					+0	28532	
g456/Y	OR2XLTS	2	0.9	1881	+8724	37256	R
fir_config_reg/power_gt_fir_3							
power_gt_fir_3	out port				+0	37256	R
(ou_del_1)	ext delay				+10000	47256	R
	path_delay					60000	

Exception : 'path_delays/del_1' 60000ps
Timing slack : 12744ps
Start-point : fir_config_reg/block_config_reg_5/CK
End-point : power_gt_fir_3

SUPR Contributions

- Scalable SoC component library
  - Provided set of blocks includes all blocks on current revision of BSN
- Simulation speedup
  - Abstraction–Accuracy–Runtime Tradeoff
- Accurate design decision automation tool
  - Representation of digital circuits in Simulink
- GUI for results feedback
- Documentation

Outline

1. Motivation and Introduction
    1. Body Sensor Nodes (BSNs)
    2. Energy Constrained SoCs
    3. Thesis and Research Goals
2. Subthreshold Digital Signal Processing (DSP)
    1. Finite-Impulse Response (FIR) Filter
    2. Fast-Fourier Transform (FFT)
    3. Approximation Techniques for FIR filter coefficients
3. **S**oC **U**ltra-Low **P**owe**R** (SUPR) Model
    1. All-Digital Phase Locked Loop (ADPLL) for clock synthesis and model validation
4. Schedule
5. Publications

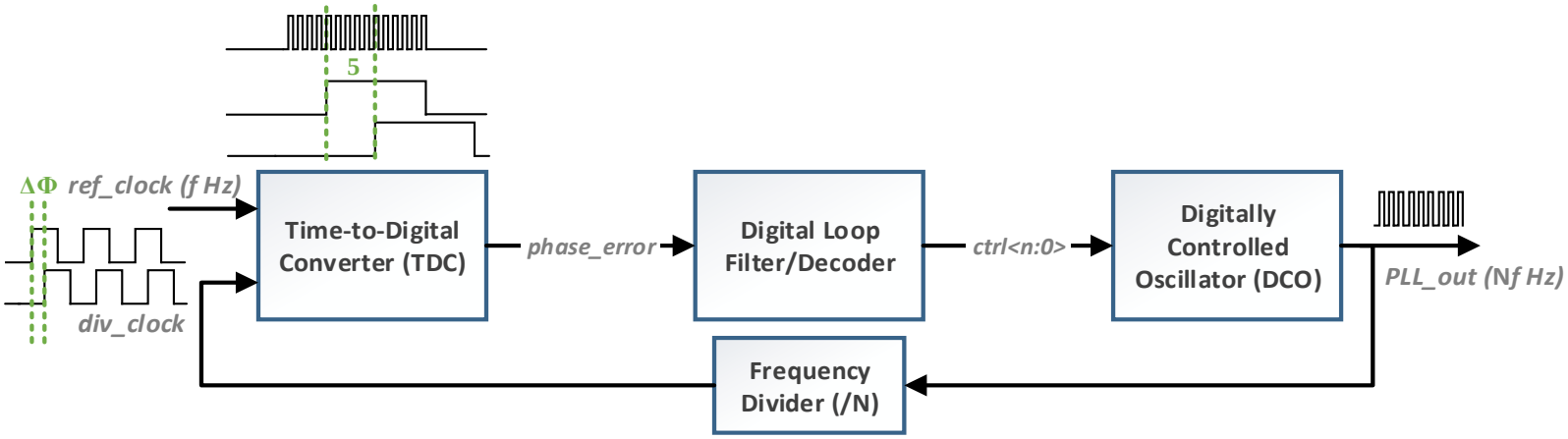
ADPLL Motivation

- Digital designs have various complexities:
  - Control logic
  - Feedback
  - Event-based operation
  - Multi-rate operation
  - Multi-domain analysis

  } ADPLL

- ADPLLs for clock synthesis
  - Clocks are always on
  - Higher frequency → high power
- No synthesizable subthreshold designs to date

ADPLL Overview



- ADPLL components
  1. Time-to-digital converter
  2. Loop Filter
  3. Digitally Controlled Oscillator
  4. Divider

Hypothesis and Metrics

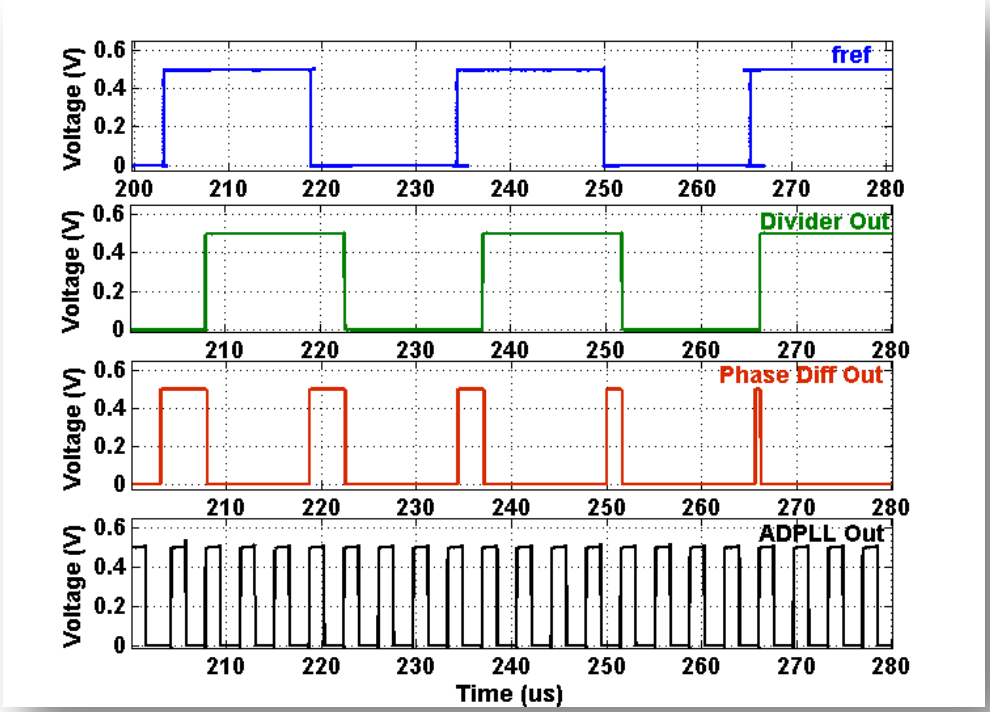
HYPOTHESIS

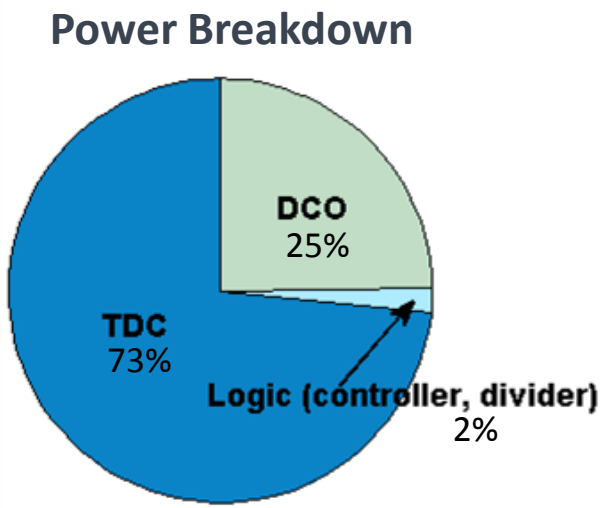
1. ADPLL is a critical system block as it's **rarely powered down**.
2. ADPLLs are well-suited for model validation due to their **representative complexity**.
3. SUPR will **provide a framework for the design and synthesis of a subthreshold ADPLL.**

METRICS

1. ADPLL Circuit
    1. Lock time
    2. Phase and Quantization noise
    3. Linear frequency range
    4. Power consumption
2. SUPR Implementation
    1. Library scalability
    2. Simulation speedup
    3. Accuracy of results
        1. Energy, Delay, Phase Noise, Lock time

Approach

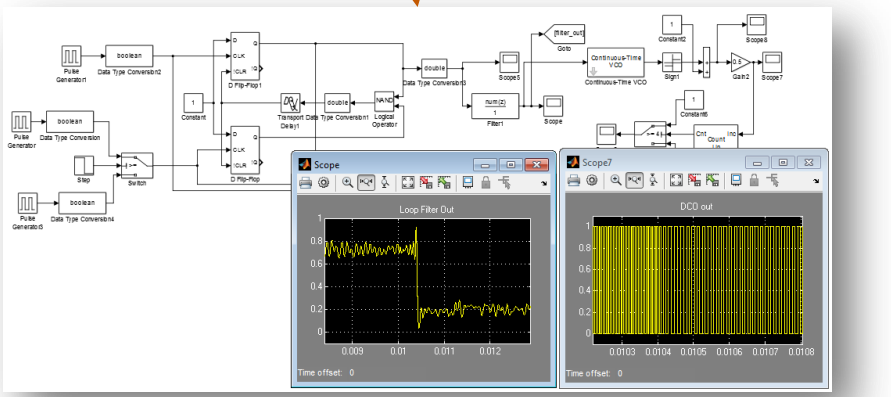




- Test chip fabricated in 130nm technology
- 32kHz → (200kHz–1MHz) using an integer–N ADPLL approach
- < 400nW simulated at 500mV
- Next iteration goal: reduce TDC power, use SUPR

ADPLL/SUPR Contributions

- Determine most energy efficient loop filter topology
  - FIR – IIR – Decoder-Based
- SUPR framework for exploring locking algorithms
- Expand SUPR library: Add synthesizable delay cell topologies
  - Inverter, tri-state
- Design and fabricate a subthreshold integer-N ADPLL
  - Validate SUPR results using SPICE/chip



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Schedule

Subject	#	Task Description	Status	Related Publications
(BSN v0) Subthreshold FIR Filter	1	Architecture Exploration	Completed	
	2	HDL Description/Simulation	Completed	
	3	Synthesis, Place and Route, Verification	Completed	
	4	Chip Testing	Completed	[AK 0][AK 1][AK 2]
BSN v1/v2	1	Chip Architecture Exploration	Completed	
	2	Block Level Architecture Explorations (FIR, FFT, Dive Profile, I2C/SPI, etc.)	Completed	
	3	HDL Description/Simulation	Completed	
	4	Synthesis, Place and Route, Verification	Completed	
	5	BSN v1 Chip Testing	Sep-13	[AK 3] [AK 4]
	6	BSN v2 Modifications	Aug-13	
	7	BSN v2 Block Synthesis/Layout	Aug-13	
	8	BSN v2 Chip Testing	Jan-14	[AK 5]
FIR Approximation	1	Architecture Choice	Completed	
	2	HDL Description/Simulation	Completed	
	3	Synthesis	Completed	
	4	Silicon Testing	Sep-13	[AK 6]
	5	Revision 2 HDL Description	May-13/Aug-13	
	6	Synthesis	May-13/Aug-13	
	7	Chip Testing	Jan-14	[AK 7]
SUPR	1	Framework Setup	Completed	
	2	Core Block Design	Completed	
	3	Library of Chip Blocks to Match BSN	Dec-13	
	4	Stateflow Integration	Jan-14	[AK 8]
	5	Statistical Integration of Energy/Delay	Feb-14	
	6	User Interface	Aug-14	
	7	Simulink-to-HDL	Jun-14	[AK 9]
ADPLL	1	Version 0 (v0) Architecture Choice	Completed	
	2	v0 HDL Description/Simulation	Completed	
	3	v0 Synthesis	Completed	
	4	v0 Chip Testing	Jun-13	[AK 10]
	5	SUPR ADPLL Framework	Nov-13	[AK 11]
	6	ADPLL v1 Design and Synthesis	May-14	
	7	ADPLL v1 Chip Testing	Dec-14	[AK 12]
Thesis Writing	1	Write final publications, await decisions	Jan-15	
	2	Write Thesis	Apr-15	
	3	PhD defense	May-15	

Publications

- Completed
  - [AK 0] Klinefelter, A.; Yanqing Zhang; Otis, B.; Calhoun, B.H., "A Programmable 34 nW/Channel Sub-Threshold Signal Band Power Extractor on a Body Sensor Node SoC," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.59, no.12, pp.937,941, Dec. 2012.
  - [AK 1] Yanqing Zhang; Fan Zhang; Shakhsheer, Y.; Silver, J.D.; Klinefelter, A.; Nagaraju, M.; Boley, J.; Pandey, J.; Shrivastava, A.; Carlson, E.J.; Wood, A.; Calhoun, B.H.; Otis, B.P., "A Batteryless 19μW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications," Solid-State Circuits, IEEE Journal of , vol.48, no.1, pp.199,213, Jan. 2013.
  - [AK 2] Fan Zhang; Yanqing Zhang; Silver, J.; Shakhsheer, Y.; Nagaraju, M.; Klinefelter, A.; Pandey, J.; Boley, J.; Carlson, E.; Shrivastava, A.; Otis, B.; Calhoun, B., "A batteryless 19μW MICS/ISM-band energy harvesting body area sensor node SoC," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International , vol., no., pp.298,300, 19-23 Feb. 2012.
- Planned
  - [AK 3] Next revision BSN paper on the entire working chip
  - [AK 4] Paper on low-power accelerators and novel DSP on the BSN chip
  - [AK 5] BSN revision v2: summary of the entire chip
  - [AK 6] FIR approximation unit for sub-threshold operation in SoCs
  - [AK 7] Approximations for classical DSPs (FIR, IIR, FFT) on low-power DSPs
  - [AK 8] A model for BSN design space exploration using Simulink
  - [AK 9] An automated and high-level design flow for digital circuit design using Simulink
  - [AK 10] A Subthreshold ADPLL for low-rate Clock Synthesis on SoCs
  - [AK 11] A model for Exploring Tradeoffs of ULP ADPLLs using Simulink
  - [AK 12] A Subthreshold ADPLL for ULP Clock Synthesis with SUPR Model Support

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  - Patricia Gonzalez
  - Divya Akella
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References

1. Zhang, F., Y. Zhang, J. Silver, Y. Shakhsheer, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19uW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", ISSCC, San Francisco, 02/2012.
2. Klinefelter, A.; Yanqing Zhang; Otis, B.; Calhoun, B.H., "A Programmable 34 nW/Channel Sub-Threshold Signal Band Power Extractor on a Body Sensor Node SoC," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.59, no.12, pp.937,941, Dec. 2012.
3. Myeong-Eun H., et al., "A 85mV 40nW Process-Tolerant Subthreshold 8x8 FIR Filter in 130nm Technology," VLSI Circuits, 2007 IEEE Symposium on, June 2007.
4. Wei-Hsiang M., et al., "187 MHz Subthreshold-Supply Charge-Recovery FIR," Solid-State Circuits, IEEE Journal of, April 2010.
5. Zhang, F., et al., "A low-power multi-band ECoG/EEG interface IC," Custom Integrated Circuits Conference (CICC), 2010 IEEE, Sept. 2010.

Questions?

DCO

- Many delay cell topologies
- Want **high resolution, low locking time**